

Low-Noise VCO Runs on Low Voltage

Microwaves and RF

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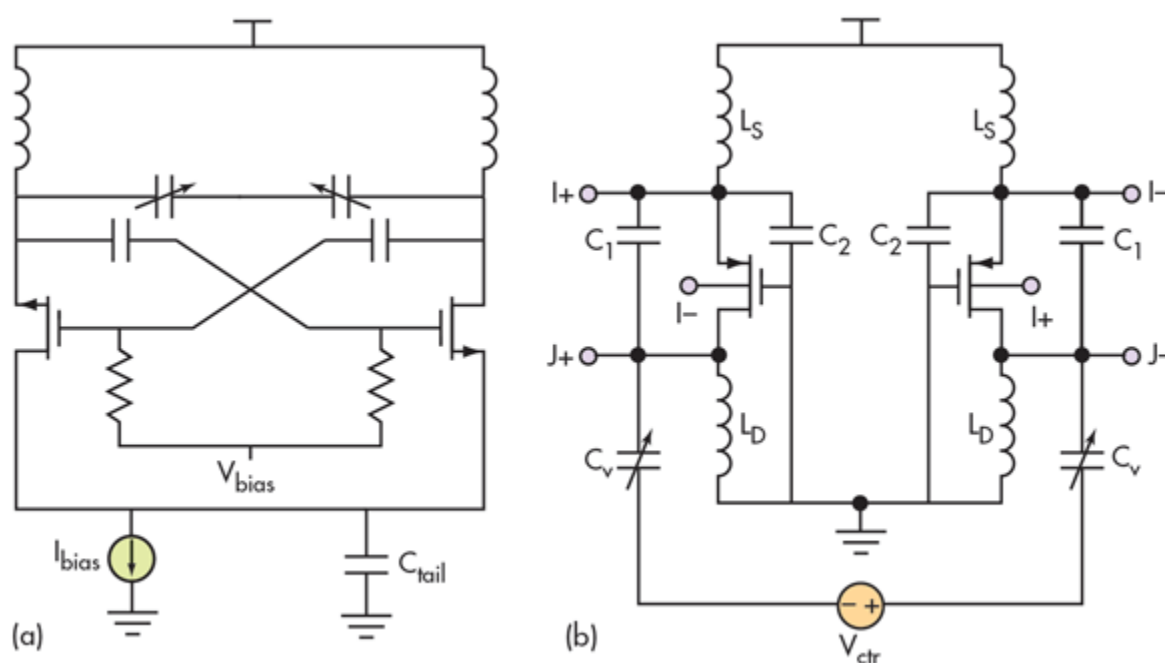
This quadrature PMOS Colpitts VCO requires very little power for stable, low-phase-noise operation at 2.4 GHz.



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Some applications must generate their signals when only low supply voltages are available, such as in battery-powered systems. Fortunately, a quadrature voltage-controlled oscillator (QVCO) has been developed that can be fabricated with p-type metal-oxide-semiconductor (PMOS) solid-state technology. It features low phase noise and low power consumption over a moderate tuning range (5% from 2.325 to 2.440 GHz).



Quadrature coupling is achieved by a direct coupling technique for a reduction in power consumption, phase noise, and chip size. Suitable for a variety of wireless communications applications, the Colpitts-topology QVCO adds capacitive feedback to achieve an enhanced voltage swing over its tuning range. The prototype QVCO boasts phase noise of -128.2 dBc/Hz offset 1 MHz from a 2.34-GHz carrier while consuming only 0.535 mW power from a +0.55-VDC supply.

Quadrature signals play an important role in both wireless and wireline communication systems. They are used in a variety of different analog and digital modulation schemes, and several techniques can be employed to produce quadrature signals. For example, a VCO with a doubled frequency followed by a divide-by-two circuit can be used, as can a polyphase filter or a QVCO.¹ QVCOs have been shown to be critical components in applications that require high-fidelity quadrature signals—certain communications transceivers, for example

nce they can generate quadrature signals with superior phase noise and low power consumption. But ignoring a source capable of high-spectral-purity quadrature signals with low power consumption is still a challenge.

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The simplest and most convenient way to implement a QVCO is by coupling two symmetric inductive-capacitive (LC) tank VCOs.²⁻⁴ The main drawback to this approach is the typically poor phase noise that results. In 2008, a Class-C VCO topology was proposed with a theoretical phase-noise improvement of 3.9 dB for the same current consumption as a standard differential-pair LC tank oscillator.⁵ Following that approach, several new Class-C VCO topologies have been proposed.⁵⁻¹⁰ However, all of these designs are based on a single differential pair configuration, similar to a traditional VCO topology.⁵

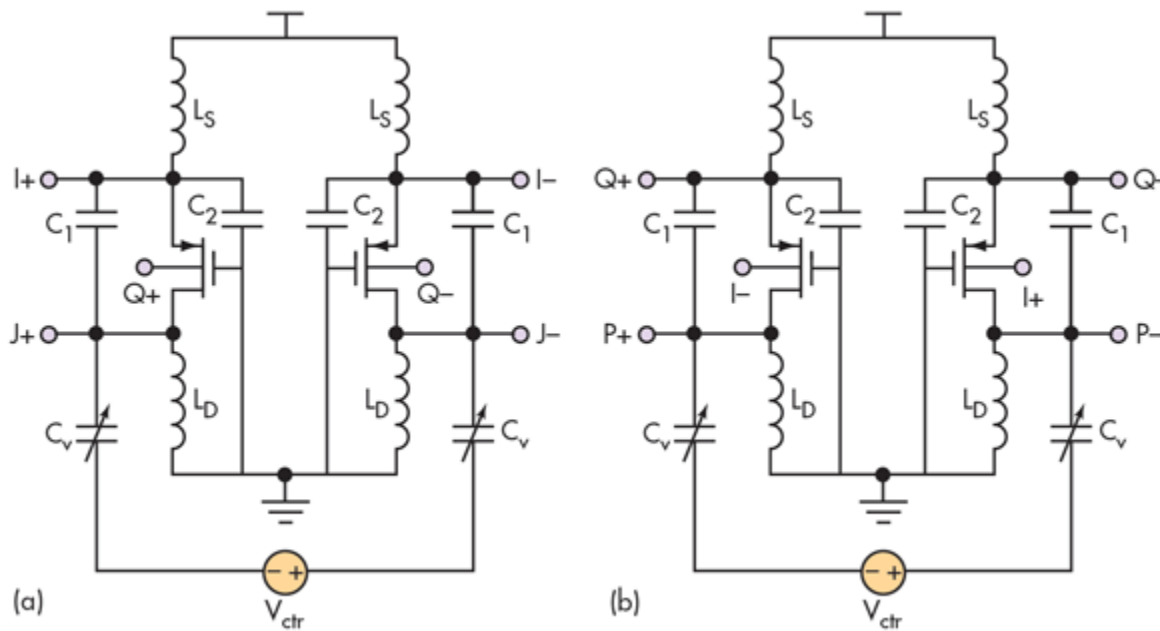
In quest of quadrature signals with low noise at low power levels, a new oscillator configuration was explored. In contrast to VCOs with traditional cross-coupled differential-pair LC-tank topologies, this new approach is a PMOS Colpitts QVCO. By employing a direct bulk coupling technique, this novel QVCO topology enables quadrature coupling without requiring additional transistors. In addition, it provides an enhanced voltage swing under a low supply voltage by means of a capacitive feedback technique.

Figure 1(a) shows a cross-coupled, differential-pair, Class-C oscillator. Bias current is inserted between the NMOS source and ground and, in most cases, this is accomplished by means of a tail transistor. To filter high-frequency noise from the bias current, a large tail capacitance is employed; together with an resistive-capacitive (RC) bias network, this can prevent the transistors from working in the deep triode region.⁵

Figure 1(b) shows the new PMOS Colpitts VCO architecture. For a given amount of current, NMOS transistors are smaller than PMOS transistors for the same value of transconductance. However, PMOS transistors exhibit about 10-dB less 1/f noise compared with NMOS transistors. PMOS transistors also feature lower hot-carrier-induced white noise than NMOS transistors. As a result, PMOS-based VCOs can achieve better phase-noise performance than NMOS-based VCOs.¹¹ Based on these considerations, a new VCO core was designed using a full PMOS transistor architecture.

Rather than using transistors (and their noise contributions) for quadrature signal coupling, direct bulk coupling is employed in this new QVCO to improve phase-noise performance while reducing power consumption and semiconductor chip area. To improve the oscillator's voltage swing while operating with a low supply voltage, capacitive feedback is employed. The typical source of bias current has been replaced by an on-chip inductor, L_D , leaving maximum voltage headroom for the oscillating signal and dramatically reducing the phase noise.¹² This technique is especially useful in low-supply-voltage topologies.

Compared to the oscillator in *Fig. 1(a)*, the proposed QVCO has eliminated bias voltage V_{bias} and the bias circuitry resistances, improving the robustness of the new oscillator's startup functionality and reducing the thermal noise of said bias resistances. To improve QVCO startup, feedback capacitor C_2 has been inserted between the PMOS source and gate. The greatest difference between the new QVCO topology of *Fig. 1(b)* and the traditional topology of *Fig. 1(a)* is that the new design employs a Colpitts architecture instead of the traditional cross-coupled differential-pair LC tank topology.



The greatest difference between the proposed QVCO and the traditional cross-coupled differential-pair LC-tank configuration of *Fig. 1(a)* is the use of the Colpitts architecture in the QVCO. *Figure 2* presents a block diagram of the new PMOS QVCO. The four (quadrature) output ports are represented by parameters J+, J-, P+, and P-. Capacitive feedback is provided by capacitors C_1 and C_v . Following the pioneering work of Hsieh and Lu,¹³ a simplified expression of the QVCO voltage swing for this oscillator can be represented by Eq. 1:

$$A \approx (1 + C_1/C_v)V_{DD} \quad (1)$$

As the simulations of the traditional VCO and the QVCO will attest, the use of capacitive feedback can greatly improve the output swing of a VCO—even when it is operating at low supply voltages.



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A Closer Look



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Several methods are available for achieving quadrature coupling. These include parallel-coupled QVCOs, series-coupled QVCOs, and back-gate-coupled QVCOs.¹⁴⁻¹⁶ For the new QVCO, quadrature coupling was accomplished by means of a bulk coupling technique, whereby an additional transistor or capacitor was not needed to provide the coupling. The use of direct bulk coupling can reduce the supply-voltage requirements.

For a MOSFET device, the threshold voltage is governed by the body effect¹⁷:

$$V_t = V_{t0} + \gamma[(|2\Phi_F + V_{SB}|)^{0.5} - (|2\Phi_F|)^{0.5}] \quad (2)$$

where:

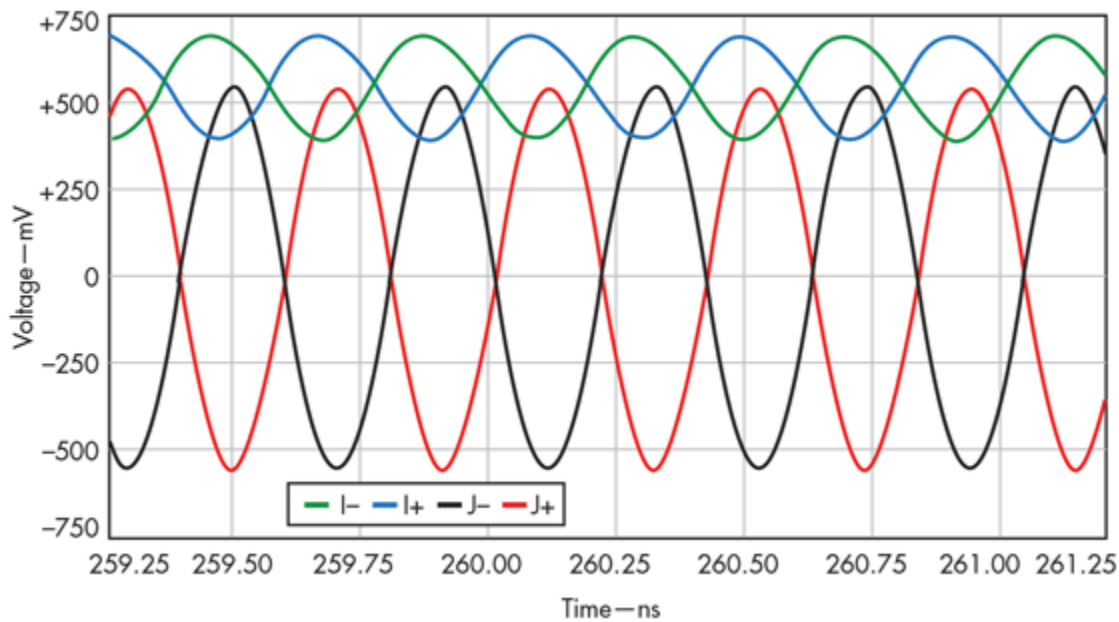
V_{SB} = the sideband voltage;

V_{t0} = the threshold voltage for $V_{SB} = 0$ V;

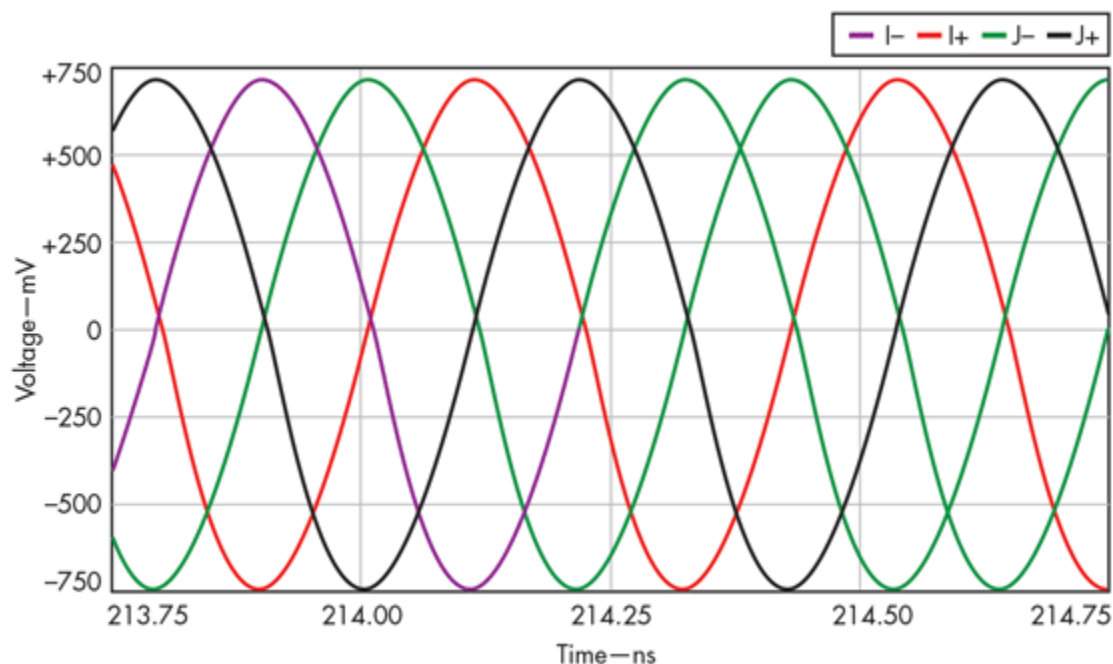
γ = the bulk effect parameter, with a typical value between 0.3 and 0.4 $V^{0.5}$; and

Φ_F = a physical parameter with typical value of 0.3 V.

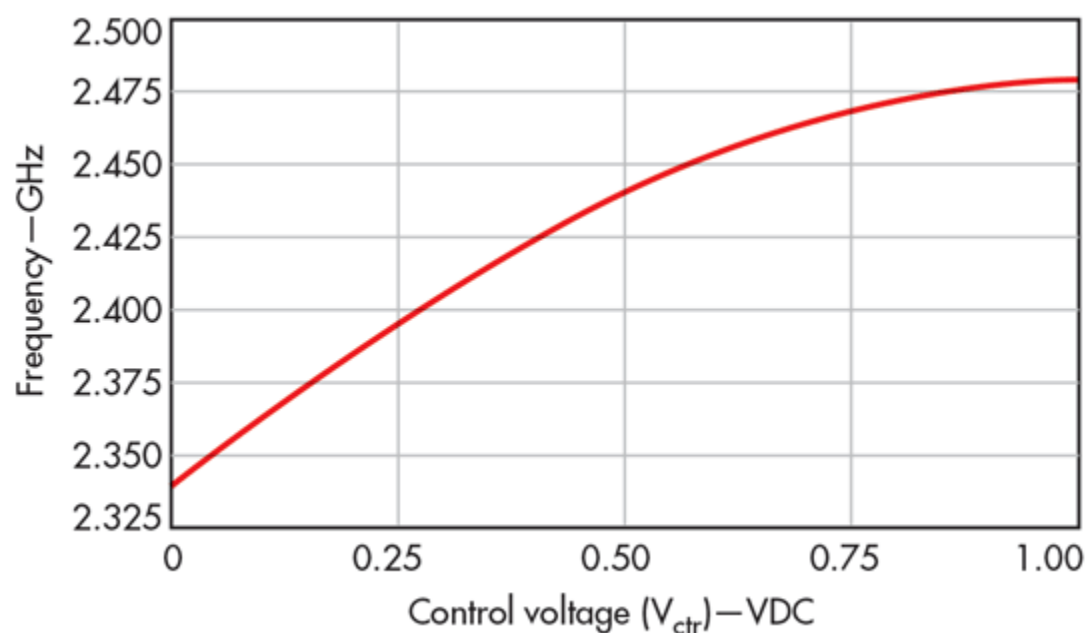
From Eq. 2, it is known that by applying both DC and AC bulk coupling, the effective threshold voltage can be reduced; this is desirable for achieving a low-supply-voltage, low-power oscillator design. Since forward biasing of the bulk coupling also helps to reduce flicker noise in a PMOS VCO, the use of bulk coupling leads to a coupling factor of less than unity.¹⁸ As a result, the direct bulk coupling technique can also improve the oscillator's phase-noise performance. The design parameters for the QVCO are as follows: $C_1 = 429.4$ fF; $C_2 = 664.9$ fF; $L_S = L_D = 7.1$ nH; and dimensional parameters of 120/0.18 μm for M_1 , M_2 , M_3 , and M_4 .

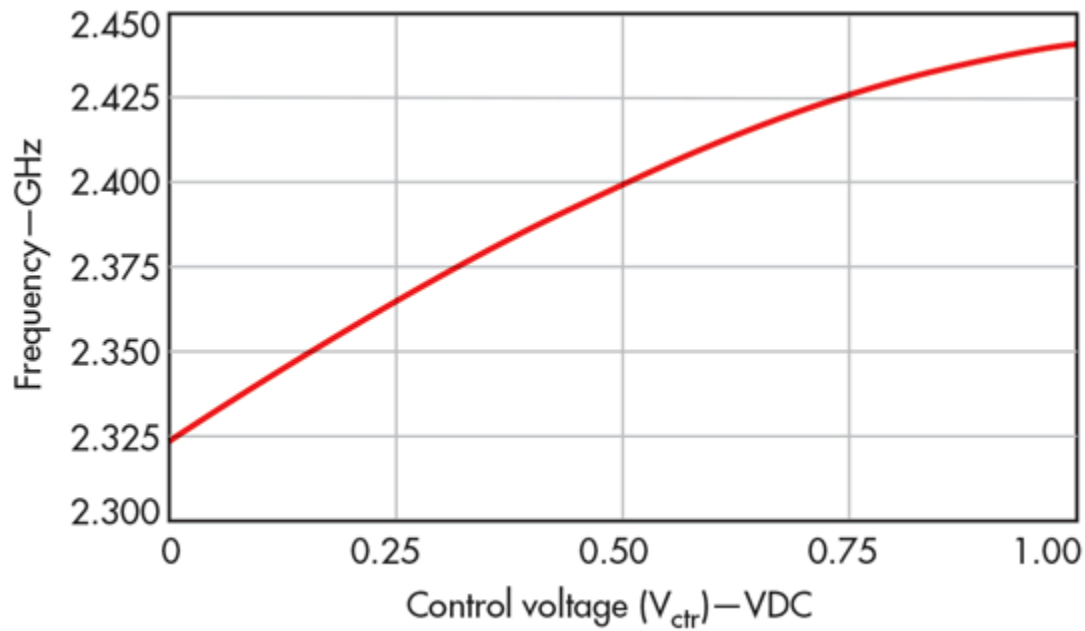


By way of comparison, circuits for the traditional VCO and the proposed PMOS Colpitts QVCO were fabricated in monolithic form using 0.18- μm RF CMOS semiconductor technology from [Taiwan Semiconductor Manufacturing Company Ltd. \(TSMC\)](http://www.tsmc.com). The two oscillator circuits were compared in terms of output voltage swing, frequency tuning range, and phase noise. *Figures 3 and 4* show the output voltage swings of the standard VCO and the PMOS QVCO cores, respectively.

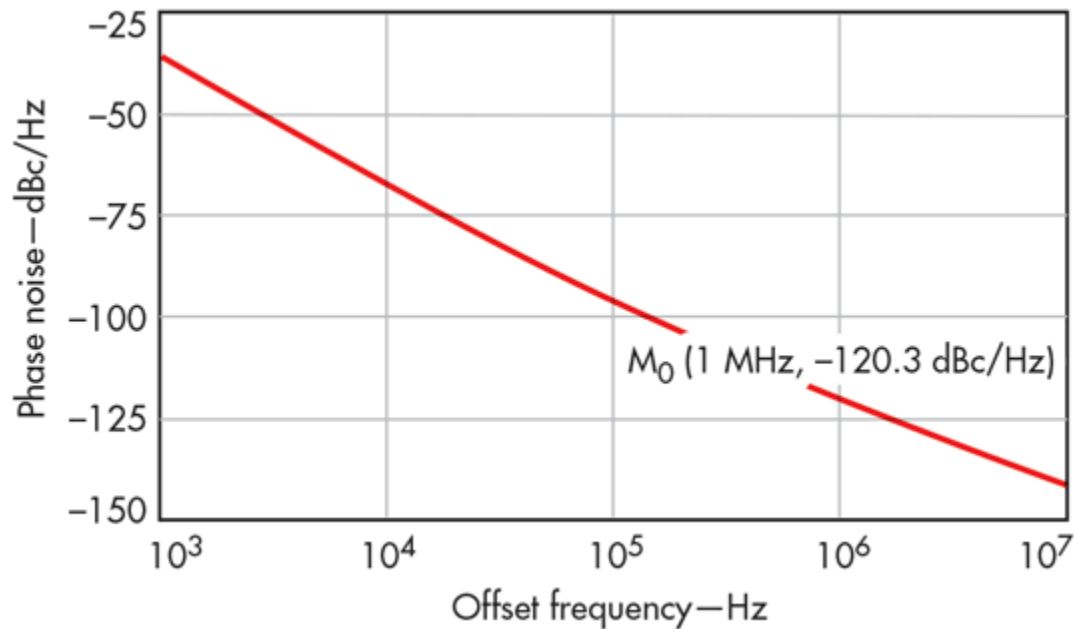


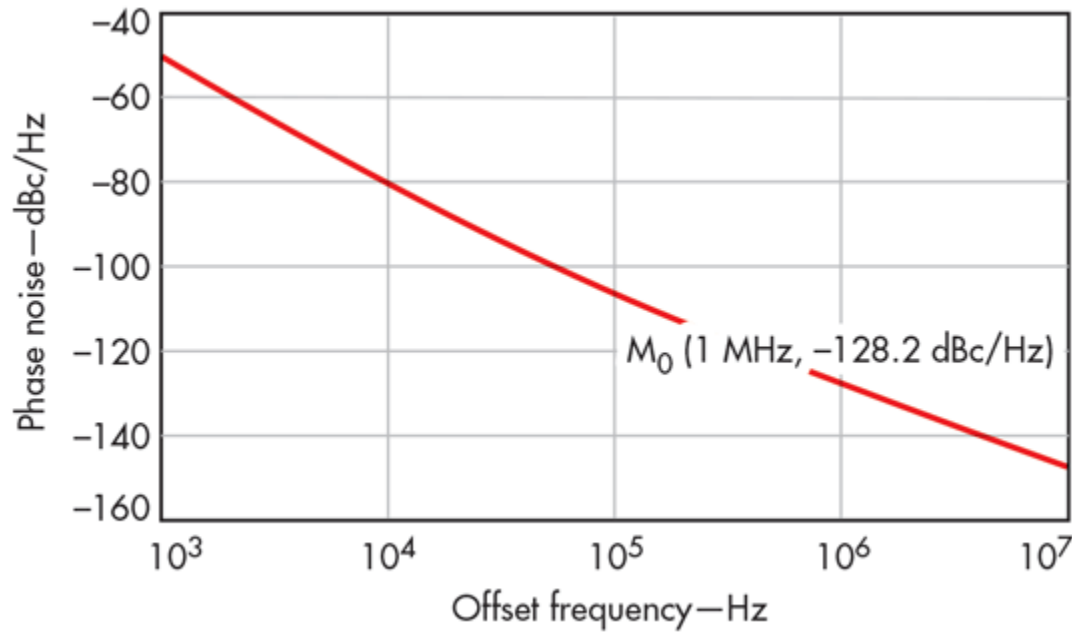
As the plots reveal, the standard VCO circuit draws DC current of $486\ \mu\text{A}$ when operating with a $+0.55\text{-VDC}$ supply while the QVCO draws a higher $972\ \mu\text{A}$ when running on the same $+0.55\text{-VDC}$ supply voltage. From *Fig. 3*, it is known that the J- and J+ ports deliver higher output swings than the I- and I+ ports.





Figures 5 and 6 display the tuning ranges of the two oscillator architectures. The frequency range of the standard VCO is 2.34 to 2.48 GHz when control voltage V_{ctr} sweeps from 0 to +1 VDC; the tuning range of the QVCO is 2.325 to 2.440 GHz when working with the same V_{ctr} range. Figures 7 and 8 offer phase-noise performance levels for the two oscillator architectures. As these plots show, the best phase noise for the traditional VCO is -120.3 dBc/Hz offset far (1 MHz) from the carrier while the phase noise for the proposed QVCO is as low as -128.2 dBc/Hz offset 1 MHz from the carrier. In general, the performance of the new QVCO is superior to that of the traditional VCO, except for power consumption.





A figure of merit (FOM) was employed to evaluate the three performance parameters of frequency, phase noise, and power dissipation for the QVCO, as detailed in Eq. 3:

$$\text{FOM} = \text{ELL}(f_{\text{offset}}) - 20\log(f_o/f_{\text{offset}}) + 10\log(\text{PDC}/1 \text{ mW}) \quad (3)$$

where:

PDC = the power dissipated by the oscillator core (in mW);

ELL(f_{offset}) = the phase noise at the oscillator carrier frequency;

f_{offset} = the offset frequency from the oscillator carrier; and

f_{offset} = the center frequency.

The performance of the new QVCO is summarized in the *table*, and compared with recent work in QVCOs. The new low-voltage design exhibits the best FOM among these reported QVCOs, with higher FOM values indicating better oscillator performance.

COMPARING QVCO PERFORMANCE WITH RECENT RESULTS						
Reference	Technology (nm)	V _{DD} (V)	Tuning range (GHz)	Power (mW)	Phase noise (dBc/Hz at 1 MHz offset)	Figure of merit
1	130	0.6	5.4 to 5.62	4.2	-122	-191.4
19	130	1.2	2.9 to 5.4	9.8	-123.3 at 2 MHz	-190
20	180	1.0	2.6 to 3.19	1.57	-123	-191.1
21	180	1.8	6.09 to 7.5	2.16	-123 at 2 MHz	-191
22	180	1.2	4.74 to 4.85	3.4	-125	-193
Proposed QVCO	180	0.55	2.325 to 2.44	0.535	-128.2	-198.3

In summary, a new PMOS Colpitts QVCO for a +0.55-VDC supply voltage has been developed and fabricated with a commercial 0.18- μm silicon CMOS technology. By using capacitive feedback and a direct bulk coupling technique, the quadratic oscillator achieves significant improvements in terms of power consumption and phase-noise performance, making it an attractive candidate for low-power RF/microwave applications requiring low supply voltages.

On the negative side, the proposed QVCO topology requires eight inductances, which leads to a larger required chip area than some other QVCO topologies. The four tail inductances, L_s , can be replaced by resistances or MOSFETs, but simulations show that this will degrade the phase-noise performance and power consumption. It will also require the use of a larger supply voltage, revealing the tradeoff of supply voltage, power consumption, phase noise, and chip area for this new QVCO design.



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